## REMARKS

Applicants respectfully traverse and request reconsideration.

Applicants wish to thank the Examiner for the notice that claims 7-13 and 20-27 would be allowed if amended to overcome the typographical error and that claims 15-17 would be allowed if written in independent form including all of the limitations of the base claim and any intervening claims.

Claims 7-13 and 20-27 stand rejected under 35 U.S.C. §112, 2 para., as being indefinite for failing to particularly point out and distinctly claim the subject matter which Applicants regard as the invention due to a typographical error regarding the words "the information". Applicants have corrected the typographical error and as such Applicants respectfully request that this rejection be withdrawn.

Claims 1-4, 14, 18, 19, 20-31 stand rejected under 35 U.S.C. §103(a) as being unpatentable over Wandler (U.S. Patent No. 5,991,833) in view of Connors et al. (U.S. Patent No. 4,152,764). The Wandler reference is directed to a computer system with bridge logic that attempts to reduce interference to CPU cycles during secondary bus transactions. The computer system includes a CPU and memory device coupled through a north bridge logic device. The computer also includes a south bridge logic device coupled to the north bridge by a primary bus. The south bridge waits as long as possible before asserting a flush request control signal to the north bridge. The south bridge asserts the flush request signal to the north bridge after a peripheral device coupled to the south bridge requests access to the primary bus to run a cycle. In an alternative embodiment, the invention includes a pair of south bridges wherein one south bridge is in a laptop computer and another south bridge is in an expansion base to which the laptop computer mates. The Wandler reference makes passing reference in column 6, lines 5-7 that the bridge logic 50 may be integrated into the CPU 25 but does not appear to describe how





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this would be done. In any event, the office action alleges that the Wandler reference teaches all of the elements of claims 1 and 28 but fails to disclose that memory access requests are processed by the north bridge at a rate of memory. Connors has allegedly been cited for this proposition.

However, the Connors reference is directed to a flowing priority storage control for processors in a multi-processor system. Shared storage access is controlled in each processor by means of a multi-processor priority pointer circuit that receives storage requests granted by a local priority circuit in the processor. The MP priority pointer circuits are interconnected between the processors and when a burst ends for one processor, another processor having one or more pending storage requests is given priority and begins its burst during the missed cycle. Priority flips back and forth between the processors as they access main storage in bursts of requests. Connors does not appear to be directed to a system that employs north bridges or south bridges as claimed nor to integration of a north bridge and central processing unit is claimed. As such, it appears that Applicants' claimed invention and the cited reference appear to be directed to different problems and different structure. Moreover, the cited portion of Connors does not appear to teach what the office action alleges.

For example, the office action cites column 2, lines 13-27 and column 5, lines 60-67 as allegedly teaching the missing subject matter of Applicants' claimed invention in claim 1, namely processing, by the north bridge, the memory access requests at a rate of memory. However, as noted, there is no north bridge disclosed in the Connors reference in the cited portions nor do the cited portions appear to teach processing memory access requests by the north bridge at a rate of memory. The cited portions refer to multiple processors, each being identical models and controlling the processors so that their sum of storage access rates equals





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100% of the storage access cycle rate of the main storage. Applicants' claim 1, for example, is not directed to a multiple processor system that attempts to allow the sum of multiple processors to equal maximum storage access rate. To the contrary, the Applicants' invention claims that the rate from the north bridge of memory requests to the memory is at the memory rate and not at a lower rate as apparently taught by the Connors reference. In addition, it appears that the Connors reference actually teaches away from Applicants' claimed invention in that in column 5, lines 49-54 Connors notes that it is a characteristic of a single processor not to be able on a long term basis to continuously input requests to a circuit at the storage access rate, because after a short period of time, either the required logical storage units are found unavailable or the request buffers are empty. In contrast, Applicants claim that the north bridge processes memory on access requests at the rate of the memory. Connors teaches that a multiple processor system is necessary with a priority based access control scheme to facilitate efficient memory access.

Applicants also respectfully submit that the motivation supplied in the office action, if assumed to be true, would not result in the Applicants' claimed invention. For example, the office action indicates that it would have been obvious to one of ordinary skill in the art to use Connors in the Wandler system for processing a request at a memory rate because Connors could provide Wandler the controllability to adjust memory width and read write cycles such that memory requests at a given memory speed could be processed by Wandler. However, Connors actually teaches using multiple processors to gain access to memory and controlling each of those processors access at different speeds or allow each processor independently to access in burst fashion giving priority to a specific processor. For argument sake, if the teaching of Connors are combined with those of Wandler, as best understood, the resulting system would be one in which the sum of the rates of access by a plurality of processors would equal 100% over a

long period of time for the main memory. This is contrary to Applicants' claim language which requires that the north bridge process the memory access requests at the rate of memory. The claim does not recite that the memory is accessed at varying rates that when combined equal 100% of a rate of memory as required in the Connors reference. Accordingly, Applicants respectfully submit that the claims are in condition for allowance.

In addition, as to claim 28, the office action cites the combination of Wandler and Connors but does not appear to address the limitation that the south bridge is also integrated. As such, this claim is also believed to be in condition for allowance.

As to claim 2, it is alleged that Wandler teaches integrating the south bridge on the substrate with a CPU in the north bridge. However, the cited section, namely column 6, lines 5-7, refer specifically only to the north bridge and it does not appear that Wandler contemplates integrating both a north bridge and south bridge on the same chip. In fact, Wandler teaches using a pair of south bridges that are actually in different products. Accordingly, this claim is also believed to be in condition for allowance. Again, Applicants respectfully note that the Wandler reference appears to teach that the memory is in fact off chip. As such, column 6, lines 1-27 appear to fail to teach the claimed invention.

As to claim 4, the cited portion of the reference, namely column 6, lines 28-52, appear to be silent as to integrating a graphics controller on the substrate with the central processing unit and the north bridge and bypassing an AGP request and transforming them into memory requests as required by the claim. Accordingly, this claim is also believed to be in condition for allowance.

As to claim 14, Applicants respectfully reassert the relevant remarks made above.





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The other dependent claims also add additional novel and nonobvious subject matter and are also believed to be in condition for allowance.

Claims 5, 6, 32 and 33 stand rejected under 35 U.S.C. §103 as being unpatentable over Wandler in view of Connors and further in view of Onishi et al. (U.S. Patent No. 5,845,329). Applicants respectfully reassert the relevant remarks made above and as such these claims are also believed to be in condition for allowance. Applicants also respectfully submit that the Onishi reference, namely column 10, lines 4-13 do not appear to describe translating, by the north bridge, the address for virtual memory space to an address in physical memory space since a north bridge does not appear to be discussed in the cited section. As such, the claims are also believed to be allowable for this reason also.

Accordingly, Applicants respectfully submits that the claims are in condition for allowance and respectfully request that a timely Notice of Allowance be issued in this case. The Examiner is invited to contact the below-listed attorney if the Examiner believes that a telephone conference will advance the prosecution of this application.

Respectfully submitted,

Date: 1/28/04

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